REMARKS

Prior to the present amendment and response, claims 1-20 were pending in the present application. By the present amendment, claims 1, 8, and 15 have been amended and claims 2-5, 9-13, and 17-18 have been canceled. Thus, claims 1, 6-8, 14-16, and 19-20 remain in the present application. Withdrawal of the present final rejection and reexamination and allowance of pending claims 1, 6-8, 14-16, and 19-20 in view of the above amendments and the following remarks are respectfully requested.

A. Double Patenting Objection to Claims 8-14

The Examiner had objected to original claims 8-14 under 37 CFR §1.75 as resulting in a potential "double patenting" of original claims 1-7. Applicant respectfully submits that the amended claims overcome the Examiner's double patenting objection.

B. Rejection of Claims Under 35 USC §102(b) and 35 USC §103(a)

The Examiner has rejected original claims 1, 6-8, and 13-14 under 35 USC §102(e) as being anticipated U.S. Patent Application Publication No. 2005/0079696 to Colombo (hereinafter "Colombo"). Original claims 2-5, 9-12, and 15-20 have been rejected under 35 USC §103(a) as being unpatentable over Colombo in view of U.S. Patent No. 6,265,260 to Alers et al. (hereinafter "Alers"), U.S. Patent No. 6,566, 250 to Tu et al. (hereinafter "Tu"), or U.S. Patent No. 6,162,717 to Yeh (hereinafter "Yeh"). Claims 1, 7-8 and 14 have been separately rejected under 35 USC §102(b) as being

anticipated U.S. Patent No. 5,891,798 to Doyle et al. (hereinafter "Doyle"). Claims 2-6, 9-13, and 15-20 have also been separately rejected under 35 USC §103(a) as being unpatentable over Doyle in view of Alers, Tu, or Yeh. For the reasons that follow, Applicant submits that the present invention, as defined by amended independent claims 1, 8, and 15, is patentably distinguishable over the cited references, either singly or in combination.

By reference to Figures 1 and 2 of the present application, the present invention performs a nitridation process on gate stack 102 immediately after the gate etch process has been performed. By performing the nitridation process to nitridate sidewalls 110 of gate stack 102 after the gate etch process has been performed, the present invention's process flow can utilize the nitridation process to repair damage that may occur to gate stack 102 during the gate etch process. Additionally, during the nitridation process, nitrogen is introduced into high-k dielectric segment 106. As a result, the nitrogen that is introduced into high-k dielectric segment 106 can form a barrier that can prevent undesirable lateral oxygen diffusion into high-k dielectric segment 106 during subsequent processing steps. In an embodiment of the present invention that utilizes a gate stack comprising an interfacial layer, where the interfacial layer comprises nitride, the nitridation process can replace nitride that has been depleted in the interfacial layer during the gate etch process. *See, e.g., page 8 of the present application, lines 9-21.* Moreover, as now required by the amended independent claims, the processes of etching the gate stack and the nitridation of the etched gate stack is performed in a single process

chamber. *See, e.g., page 9 of the present application, lines 20-22.* Utilization of a single process chamber has a number of advantages; for example, there will be no need to break vacuum and, thus, throughput is increased and manufacturing costs are reduced.

Colombo describes an encapsulated MOS transistor gate structures and methods for making the same. According to Colombo, sidewalls of patterned gate structures are conditioned by nitriding the sidewalls of the gate structure, and a silicon nitride encapsulation layer is formed to protect the conditioned sidewalls during manufacturing processing. The conditioning and encapsulation avoid oxidation of metal gate layers, and also facilitate repairing or restoring stoichiometry of metal that may be damaged or altered during gate patterning. *See, Figures 4, and 5G through 5L of Colombo.*

However, as the Examiner has acknowledged, Colombo does not teach, disclose, or suggest utilizing plasma, much less using the same plasma chamber for both the gate etch and nitridation processes as disclosed and claimed by the present invention. *See, e.g., page 4 of the present Office Action, lines 5-7.* However, the Examiner has stated that any of the cited references Alers, Tu, or Yeh can be used to cure this deficiency of Colombo. *See, e.g., page 4 of the present Office Action, lines 7-9.*

Alers is directed to a method for making a capacitor by forming a first metal electrode comprising a metal nitride surface and a tantalum pentoxide layer on the metal nitride surface while maintaining a temperature below an oxidizing temperature of the metal, and remote plasma annealing the tantalum pentoxide layer. *See, e.g., column 1, line 62 through column 2, line 54 of Alers.* Thus, Alers does not remotely suggest

application of its disclosure to plasma nitridation of gate stacks in transistors after the gate etch.

Moreover, Tu is directed to forming a self-aligned capping layer over a metal filled feature in a semiconductor device by blanket deposition of a first barrier layer over an anisotropically etched feature to prevent diffusion of metal into the substrate; filling the anisotropically etched feature with a metal to form a metal filled feature filled with metal; planarizing the substrate surface to form an exposed surface of the metal filled feature; and depositing a second barrier layer to cover the exposed surface of the metal filled feature to form a capping layer. *See, e.g., column 3, lines 37-53 of Tu.* Thus, Tu does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after the gate etch.

Further, Yeh discloses a method involving fabrication of a gate structure over a semiconductor substrate and then treating the sidewalls of the gate structure with nitrous oxide plasma so that the silicon and tungsten atoms within the gate structure can react with activated nitrogen in the plasma to form chemical bonds. Thereafter, spacers are formed over a sidewall oxide layer. *See, e.g., column 2, lines 31-57 of Yeh.* However, Yeh does not suggest that the processes of etching the gate stack and the nitridation of the etched gate stack are performed in a single plasma chamber.

Doyle has been cited as anticipating the original claims, or making the claims obvious in view of Alers, Tu, or Yeh. However, Doyle discloses a method for increasing the dielectric constant of a gate dielectric by using a high dielectric constant material,

such as a paraelectric material, instead of silicon dioxide. First, nitrogen is implanted into the silicon through a sacrificial oxide layer. After annealing the substrate and stripping the sacrificial oxide, a dielectric layer is formed from a material with a high dielectric constant, such as a paraelectric material. Although the paraelectric material provides a source of oxygen for oxidation of silicon in subsequent high temperature process steps, Doyle claims that no oxidation takes place due to the presence of the nitrogen in the silicon. Therefore, there is no undesired decrease in the overall capacitance of the dielectric. When a gate electrode is formed on the dielectric layer, a nitrogen implant into the gate electrode can be used to prevent oxidation at the upper interface of the gate dielectric. *See, e.g., column 2, line 48 through column 3, line 44 of Doyle.* However, Doyle does not suggest that the processes of etching the gate stack and the nitridation of the etched gate stack are performed in a single plasma chamber. Moreover, as discussed above, use of a single plasma nitridation process chamber is not suggested by Alers, Tu, or Yeh. Thus, amended independent claim 1 is patentably distinguishable over each primary reference Colombo or Doyle singly, or in any of their respective combinations with secondary references Alers, Tu, and Yeh.

C. Conclusion

For the foregoing reasons, amended independent claim 1 is patentably distinguishable over the cited art. Furthermore, amended independent claims 8 and 15 now contain limitations in addition to those in amended independent claim 1. As such,

amended independent claims 8 and 15 are also patentably distinguishable over the cited art. Moreover, the pending dependent claims are also distinguishable over the cited art for the reasons discussed above and also for additional limitations contained in each dependent claim. Thus, it is submitted that all claims 1, 6-8, 14-16, and 19-20 remaining in the present application are in condition for allowance, and an early notice of allowance directed to all pending claims 1, 6-8, 14-16, and 19-20 is respectfully requested.

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Respectfully Submitted,
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